SECTION II—CLAIMS

1. (Previously Presented) A method comprising:

issuing a plurality of commands to a controller, wherein the commands are issued in a first order; and

indicating the completion status of commands in a second order, wherein the second order is different from the first order.

2. (Original) The method of claim 1 wherein each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command.

3. (Original) The method of claim 2 wherein the memory address included in the command is an absolute address.

4. (Original) The method of claim 2 wherein the memory address included in the command is an offset from a base memory address.

5. (Original) The method of claim 1 wherein each command is stored in a first memory location, and the completion status of each command is written to a second memory location different from the first memory location.

6. (Original) The method of claim 1 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

7. (Original) The method of claim 6 wherein the commands are grouped into categories depending on their execution times.

8. (Original) The method of claim 6 wherein the commands are grouped into categories depending on which of a plurality of resources executes them.

9. (Original) The method of claim 6 wherein each block of memory comprises a plurality of memory locations.

10. (Original) The method of claim 6 wherein each block of memory comprises a single memory location.

11. (Original) The method of claim 2 wherein the value to be written indicates the command's original location.

12. (Previously Presented) An article of manufacture, comprising:

a machine-readable medium having instructions stored thereon to:

issue a plurality of commands from a controller, wherein the commands are issued in a first order; and

indicate the completion status of commands in a second order, wherein the second order is different from the first order.

13. (Original) The article of manufacture of claim 12 wherein each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command.

14. (Original) The article of manufacture of claim 13 wherein the memory address included in the command is an absolute address.

15. (Original) The article of manufacture of claim 13 wherein the memory address included in the command is an offset from a base memory address.

16. (Original) The article of manufacture of claim 13 wherein the value to be written indicates the command's original location.

17. (Original) The article of manufacture of claim 12 wherein each command is stored in a first memory location, and the completion status of each command is written to a second memory location different from the first memory location.

18. (Original) The article of manufacture of claim 12 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

19. (Original) The article of manufacture of claim 18 wherein the commands are grouped into categories depending on their execution times.

20. (Original) The article of manufacture of claim 18 wherein the commands are grouped into categories depending on which of a plurality of resources executes them.

21. (Original) The article of manufacture of claim 18 wherein each block of memory comprises a plurality of memory locations.

22. (Original) The article of manufacture of claim 18 wherein each block of memory comprises a single memory address.

23. (Previously Presented) An apparatus comprising:

a controller adapted to accept a plurality of commands, wherein the commands are issued in a first order; and

wherein a completion status of each command is indicated in a second order, and wherein the second order is different from the first order.

24. (Original) The apparatus of claim 23 wherein each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command.

25. (Original) The apparatus of claim 23 wherein the commands are grouped into categories, and wherein the completion status of commands in each category are written to different blocks of memory locations.

26. (Original) The apparatus of claim 25 wherein each block of memory locations comprises a plurality of memory locations.

27. (Original) The apparatus of claim 25 wherein each block of memory locations comprises a single memory location.

28. (Previously Presented) A system comprising:

a controller adapted to accept a plurality of commands, wherein the commands are issued in a first order;

a plurality of computational units, wherein the units execute the plurality of commands; and

a memory, wherein a completion status of commands is written to the memory in a second order, and wherein the second order is different from the first order.

29. (Original) The system of claim 28 wherein each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command.

30. (Original) The system of claim 28 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

31. (Original) The system of claim 30 wherein each block of memory locations comprises a plurality of memory locations.

32. (Original) The system of claim 30 wherein each block of memory locations comprises a single memory location.